09.05.00 A

Please type a plus sign (+) inside this box → [+]

PTO/SB/05 (4/98)
Approved for use through 09/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	MI22-1518
First Inventor or Application Identifier	Vishnu K. Agarwal
Title	Capacitor Fabrication Methods and Capacitor Constructions
Express Mail Label No.	EL465688205US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [Total Pages 28] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 5]
4. Oath or Declaration [Total Pages]
   a. [ ] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [ ] Assignment Papers (cover sheet & document(s))
8. [ ] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [X] Other: Check in the amount of $876.00

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

Prior application information: Examiner _____ *Group / Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[X] *Customer Number or Bar Code Label* 021567 *(Insert Customer No. or Attach bar code label here)* *or* [ ] *Correspondence address below*

Name					
Address					
City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	James E. Lake	*Registration No. (Attorney/Agent)*	44,854
Signature	James E. Lake	*Date*	31 Aug 2000

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231.

PTO/SB/17 (12/98)
Approved for use through 9/30/2000. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

FEE TRANSMITTAL for FY 1999

Patent fees are subject to annual revision.
Small Entity payments must be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12.

TOTAL AMOUNT OF PAYMENT ($) 876.00

Complete if Known	
Application Number	Unknown
Filing Date	August 31, 2000
First Named Inventor	Vishnu K. Agarwal
Examiner Name	Unassigned
Group / Art Unit	Unassigned
Attorney Docket No.	MI22-1518

EL465688205US

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 23-0925
Deposit Account Name: Wells, St. John

[X] Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

2. [X] **Payment Enclosed:** [X] Check [ ] Money Order [ ] Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	760	201	380	Utility filing fee	690.00
106	310	206	155	Design filing fee	
107	480	207	240	Plant filing fee	
108	760	208	380	Reissue filing fee	
114	150	214	75	Provisional filing fee	

SUBTOTAL (1) ($) 690.00

2. EXTRA CLAIM FEES

	Extra Claims		Fee from below		Fee Paid
Total Claims 26	-20** = 6	X	18.00	=	108.00
Independent Claims 4	-3** = 1	X	78.00	=	78.00
Multiple Dependent				=	0.00

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	78	202	39	Independent claims in excess of 3
104	260	204	130	Multiple dependent claim, if not paid
109	78	209	39	** Reissue indenpendent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 186.00

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	0.00
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	0.00
139	130	139	130	Non-English specification	0.00
147	2,520	147	2,520	For filing a request for reexamination	0.00
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	0.00
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	0.00
115	110	215	55	Extension for reply within first month	0.00
116	380	216	190	Extension for reply within second month	0.00
117	870	217	435	Extension for reply within third month	0.00
118	1,360	218	680	Extension for reply within fourth month	0.00
128	1,850	228	925	Extension for reply within fifth month	0.00
119	300	219	150	Notice of Appeal	0.00
120	300	220	150	Filing a brief in support of an appeal	0.00
121	260	221	130	Request for oral hearing	0.00
138	1,510	138	1,510	Petition to institute a public use proceeding	0.00
140	110	240	55	Petition to revive - unavoidable	0.00
141	1,210	241	605	Petition to revive - unintentional	0.00
142	1,210	242	605	Utility issue fee (or reissue)	0.00
143	430	243	215	Design issue fee	0.00
144	580	244	290	Plant issue fee	0.00
122	130	122	130	Petitions to the Commissioner	0.00
123	50	123	50	Petitions related to provisional applications	0.00
126	240	126	240	Submission of Information Disclosure Stmt	0.00
581	40	581	40	Recording each patent assignment per property (times number of properties)	0.00
146	760	246	380	Filing a submission after final rejection (37 CFR 1.129(a))	0.00
149	760	249	380	For each additional invention to be examined (37 CFR 1.129(b))	0.00
				Other fee (specify) _____	0.00
				Other fee (specify) _____	0.00

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 0.00

SUBMITTED BY				Complete (if applicable)	
Typed or Printed Name	James E. Lake			Reg. Number	44,854
Signature	James E. Lake	Date	31 Aug 00	Deposit Account User ID	

Burden Hour Statement: This form is estimated to take 0.2 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

EL465688205US

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION FOR LETTERS PATENT

* * * * *

CAPACITOR FABRICATION METHODS AND CAPACITOR CONSTRUCTIONS

* * * * *

INVENTORS

Vishnu K. Agarwal
Garry A. Mercaldi

ATTORNEY'S DOCKET NO. MI22-1518

CAPACITOR FABRICATION METHODS AND CAPACITOR CONSTRUCTIONS

TECHNICAL FIELD

The aspects of the invention relate to capacitor fabrication methods including forming conductive barrier layers and capacitor constructions having conductive barrier layers.

BACKGROUND OF THE INVENTION

Capacitors are common devices used in electronics, such as integrated circuits, and particularly semiconductor-based technologies. Two common capacitor structures include metal-insulator-metal (MIM) capacitors and metal-insulator-semiconductor (MIS) capacitors. One important factor to consider when selecting a capacitor structure may be the capacitance per unit area. MIS capacitors may be advantageous since a first electrode as the semiconductor may be formed of hemispherical grain (HSG) polysilicon that exhibits a higher surface area in a given region compared to a planar surface of amorphous silicon. The higher surface area provides more capacitance per unit area occupied by a capacitor.

However, a high K factor (also known as dielectric constant or "κ") dielectric material may be desirable to further enhance capacitance. Ta_2O_5 is one example of a high K factor dielectric, but it inherently forms an interfacial dielectric layer of SiO_2 when formed on a capacitor

electrode comprising HSG. The interfacial dielectric exhibits a lower K factor than Ta_2O_5 and thus reduces the effective dielectric constant for the capacitor construction. Such reduction may be significant enough to eliminate any gain in capacitance per unit area otherwise achieved by using HSG instead of a planar electrode. Use of other oxygen containing high K dielectric materials has proved to create similar problems.

Because it may be desirable to provide area enhancement of an electrode in a MIM structure using HSG, one attempt at addressing the stated problem is forming a silicon nitride insulative barrier layer over the HSG. The silicon nitride barrier layer may be formed by nitridizing the silicon of the outer surface of HSG. Unfortunately, silicon nitride exhibits a K factor of only about 7, less than the K factor of some high K factor dielectrics that are desirable. Accordingly, even the silicon nitride barrier layer reduces the effective dielectric constant of the capacitor.

SUMMARY OF THE INVENTION

In one aspect of the invention, a capacitor fabrication method may include forming a first capacitor electrode over a substrate and atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer.

Another aspect of the invention may include chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by a layer of a conductive barrier material.

Also, in another aspect of the invention a capacitor fabrication method may include forming a first capacitor electrode over a substrate. The first electrode can have an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer.

A still further aspect includes a capacitor fabrication method of forming an opening in an insulative layer over a substrate, the opening having sides and a bottom, forming a layer of polysilicon over the sides

and bottom of the opening, and removing the polysilicon layer from over the bottom of the opening. At least some of the polysilicon layer may be converted to hemispherical grain polysilicon. A first capacitor electrode may be conformally formed on the converted polysilicon, the first electrode being sufficiently thin that the first electrode has an outer surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer.

Other aspects of the invention include the capacitor constructions formed from the above described methods.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is an enlarged view of a section of a semiconductor wafer at one processing step in accordance with the invention.

Fig. 2 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 1.

Fig. 3 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 2.

Fig. 4 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 3.

Fig. 5 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 4.

Fig. 6 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 5.

Fig. 7 is an enlarged view of the section of the Fig. 1 wafer at an alternate embodiment processing step subsequent to that depicted by Fig. 2 in accordance with alternate aspects of the invention.

Fig. 8 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 7.

Fig. 9 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 8.

Fig. 10 is an enlarged view of the section of the Fig. 1 wafer at a processing step subsequent to that depicted by Fig. 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Atomic layer deposition (ALD) involves formation of successive atomic layers on a substrate. Such layers may comprise an epitaxial, polycrystalline, amorphous, etc. material. ALD may also be referred to

as atomic layer epitaxy, atomic layer processing, etc. Further, the invention may encompass other deposition methods not traditionally referred to as ALD, for example, chemical vapor deposition (CVD), but nevertheless including the method steps described herein. The deposition methods herein may be described in the context of formation on a semiconductor wafer. However, the invention encompasses deposition on a variety of substrates besides semiconductor substrates.

In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above.

Described in summary, ALD includes exposing an initial substrate to a first chemical species to accomplish chemisorption of the species onto the substrate. Theoretically, the chemisorption forms a monolayer that is uniformly one atom or molecule thick on the entire exposed initial substrate. In other words, a saturated monolayer. Practically, as further described below, chemisorption might not occur on all portions of the substrate. Nevertheless, such an imperfect monolayer is still a

monolayer in the context of this document. In many applications, merely a substantially saturated monolayer may be suitable. A substantially saturated monolayer is one that will still yield a deposited layer exhibiting the quality and/or properties desired for such layer.

The first species is purged from over the substrate and a second chemical species is provided to chemisorb onto the first monolayer of the first species. The second species is then purged and the steps are repeated with exposure of the second species monolayer to the first species. In some cases, the two monolayers may be of the same species. Also, a third species or more may be successively chemisorbed and purged just as described for the first and second species.

Purging may involve a variety of techniques including, but not limited to, contacting the substrate and/or monolayer with a carrier gas and/or lowering pressure to below the deposition pressure to reduce the concentration of a species contacting the substrate and/or chemisorbed species. Examples of carrier gases include N_2, Ar, He, Kr, Ne, Xe, etc. Purging may instead include contacting the substrate and/or monolayer with any substance that allows chemisorption byproducts to desorb and reduces the concentration of a contacting species preparatory to introducing another species. A suitable amount of purging can be determined experimentally as known to those skilled in the art. Purging time may be successively reduced to a purge time that yields an increase in film growth rate. The increase in film growth rate might be an

indication of a change to a non-ALD process regime and may be used to establish a purge time limit.

ALD is often described as a self-limiting process, in that a finite number of sites exist on a substrate to which the first species may form chemical bonds. The second species might only bond to the first species and thus may also be self-limiting. Once all of the finite number of sites on a substrate are bonded with a first species, the first species will often not bond to other of the first species already bonded with the substrate. However, process conditions can be varied in ALD to promote such bonding and render ALD not self-limiting. Accordingly, ALD may also encompass a species forming other than one monolayer at a time by stacking of a species, forming a layer more than one atom or molecule thick. The various aspects of the present invention described herein are applicable to any circumstance where ALD may be desired.

Often, traditional ALD occurs within an often-used range of temperature and pressure and according to established purging criteria to achieve the desired formation of an overall ALD layer one monolayer at a time. Even so, ALD conditions can vary greatly depending on the particular precursors, layer composition, deposition equipment, and other factors according to criteria known by those skilled in the art. Maintaining the traditional conditions of temperature, pressure, and purging minimizes unwanted reactions that may impact monolayer

formation and quality of the resulting overall ALD layer. Accordingly, operating outside the traditional temperature and pressure ranges may risk formation of defective monolayers.

The general technology of chemical vapor deposition (CVD) includes a variety of more specific processes, including, but not limited to, plasma enhanced CVD and others. CVD is commonly used to form non-selectively a complete, deposited material on a substrate. One characteristic of CVD is the simultaneous presence of multiple species in the deposition chamber that react to form the deposited material. Such condition is contrasted with the purging criteria for traditional ALD wherein a substrate is contacted with a single deposition species that chemisorbs to a substrate or previously deposited species. An ALD process regime may provide a simultaneously contacted plurality of species of a type or under conditions such that ALD chemisorption, rather than CVD reaction occurs. Instead of reacting together, the species may chemisorb to a substrate or previously deposited species, providing a surface onto which subsequent species may next chemisorb to form a complete layer of desired material. Under most CVD conditions, deposition occurs largely independent of the composition or surface properties of an underlying substrate. By contrast, chemisorption rate in ALD might be influenced by the composition, crystalline structure, and other properties of a substrate or chemisorbed species.

Other process conditions, for example, pressure and temperature, may also influence chemisorption rate.

ALD, as well as other deposition methods and/or methods of forming conductive barrier layers may be useful in capacitor fabrication methods. According to one aspect of the invention, a capacitor fabrication method includes forming a first capacitor electrode over a substrate and atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer. At least one of the first or second capacitor electrodes may comprise polysilicon, preferably hemispherical grain (HSG) polysilicon. The dielectric layer may comprise oxygen. Exemplary materials for the dielectric layer include, but are not limited to, Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate (BST), or strontium titanate (ST).

Notably, the conductive barrier layer to oxygen diffusion formed over the first electrode may provide the advantage of reducing oxidation of the electrode by oxygen diffusion from an oxygen source, for example, the dielectric layer. The dielectric layer may be formed over the barrier layer, thus, the barrier layer may reduce oxygen diffusion to the first capacitor electrode. Alternatively, such a barrier layer may reduce oxygen diffusion from the first capacitor electrode or under the first capacitor electrode to the dielectric layer or second capacitor electrode.

It follows then that the barrier layer may also be formed over the capacitor dielectric layer with the second capacitor electrode over the barrier layer such that the barrier layer reduces oxygen diffusion from the dielectric layer to the second electrode. Such positioning may also reduce oxygen diffusion from over the dielectric layer to the first capacitor electrode, for example, oxygen diffusion from the second capacitor electrode. Accordingly, one aspect of the invention may include atomic layer depositing the barrier layer over the first electrode, forming the dielectric layer over the barrier layer, and atomic layer depositing another conductive barrier to oxygen diffusion over the dielectric layer.

Prior to the atomic layer depositing, it may be advantageous to clean the deposition substrate, for example, the first electrode. Cleaning may be accomplished by a method comprising HF dip, HF vapor clean, or NF_3 remote plasma. Such cleaning methods may be performed in keeping with the knowledge of those skilled in the art. Likewise, forming the first and second electrodes and dielectric layer may be accomplished by methods known to those skilled in the art and may include atomic layer deposition, but preferably other methods.

The atomic layer depositing of the barrier layer may occur at a temperature of from about 100 to about 600 °C and at a pressure of from about 0.1 to about 10 Torr. The dielectric layer may exhibit a K factor of greater than about 7 at 20 °C. Examples of suitable materials

for the barrier layer include WN, WSiN, TaN, TiN, TiSiN, Pt, Pt alloys, Ir, Ir alloys, Pd, Pd alloys, RuO_x, or IrO_x, as well as other materials. The barrier layer may have a thickness of from about 50 to about 500 Angstroms or another thickness depending on the material properties.

One consideration in selecting a material for the barrier layer is the thickness and density of the barrier layer that will be sufficient to achieve a desired level of oxygen diffusion reduction. Another factor to evaluate is that the barrier layer might be considered to form a part of a capacitor electrode when the barrier layer contacts one of the first or second electrodes since the barrier layer is conductive. Accordingly, it may be advantageous to recalculate the desired dimensions of an electrode contacted by the barrier layer accounting for the presence of the additional conductive material. Accordingly, a "conductive" material as the term is used herein designates a material exhibiting a conductivity at 20°C of greater than 10^4 microOhm^{-1} centimeter^{-1}, or preferably greater than about 10^{12} microOhm^{-1} centimeter^{-1}. Notably, such definition expressly includes "semiconductive" material in the range of about 10^4 to about 10^{12} microOhm^{-1} centimeter^{-1}. As an alternative, a "conductive" material in the present context might be viewed as a material that does not substantially impact the capacitance otherwise achieved without the material. Generally, an "insulative" material might produce a change in capacitance as such a barrier layer.

As another aspect of the present invention, a capacitor fabrication method may include forming a first capacitor electrode over a substrate, chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode, and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer. A chemisorption product of the first and second precursor layers may be comprised by a layer of a conductive barrier material. Because the chemisorption product is comprised by the barrier layer, the barrier layer may also include conductive barrier material that is not a chemisorption product of the first and second precursor layers. A capacitor dielectric layer may be formed over the first electrode and a second capacitor electrode may be formed over the dielectric layer. The various positions for the barrier layer discussed above are also applicable to the present aspect of the invention.

In forming the chemisorption product of the first and second precursor layers, the first and second precursor layers may each consist essentially of a monolayer. Further, the first and second precursor layers may each comprise substantially saturated monolayers. The extent of saturation might not be complete and yet the barrier layer will nevertheless provide the desired properties. Thus, substantially saturated may be adequate. The first and second precursor may each consist essentially of only one chemical species. However, as described above, precursors may also comprise more than one chemical species.

Preferably, the first precursor is different from the second precursor, although for some barrier layers, the first and second precursor will be the same. Examples of pairs of first and second precursors include: WF_6/NH_3, $TaCl_5/NH_3$, $TiCl_4/NH_3$, tetrakis(dimethylamido)titanium/NH_3, ruthenium cyclopentadiene/H_2O, IrF_5/H_2O, organometallic Pt/organometallic Pt. It is conceivable that more than one of the preceding pairs may comprise the first and second precursors, but preferably only one of the pairs. Additional alternating first and second precursor layers may be chemisorbed in keeping with the above aspect of the invention to achieve a desired thickness for the barrier layer.

Although ALD and/or chemisorbing first and second precursors may be suitable for forming a barrier layer, other methods may also be suitable. Accordingly, a variety of barrier layer forming techniques may be used in combination with techniques to increase electrode surface area to provide enhancement of capacitance per unit area.

In another aspect of the invention, a capacitor fabrication method can include forming a first capacitor electrode over a substrate where the first electrode has an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. One example of obtaining the inner and outer electrode surface areas involves further forming rugged polysilicon over the substrate and forming the first electrode over the rugged polysilicon. The first electrode can also be formed on the

rugged polysilicon. The rugged polysilicon can have a surface area per unit area greater than the surface area per unit area of conventionally formed polysilicon that is not converted to rugged polysilicon. A capacitor dielectric layer and a second capacitor electrode may be formed over the first electrode to produce a capacitor construction.

The first electrode can comprise TiN, as well as other materials, and may be deposited by ALD, CVD, and perhaps other methods. The rugged polysilicon can be HSG polysilicon and it can also be undoped. Thus, in the present aspect a first electrode may be formed having an outer surface area at least 30% greater the substrate outer surface area. Advantageously, the first electrode need not comprise polysilicon to accomplish the surface area enhancement. Further, it is conceivable that the first electrode can be formed over materials other than rugged polysilicon that provide enhanced surface area compared to the substrate underlying the first electrode.

To achieve more preferred first electrode surface area, rugged polysilicon may be formed using a seed density sufficiently small to yield at least some spaced apart grains. Thus, forming subsequent layers of the capacitor does not fill the space between grains so much as to reduce the capacitance enhancement possible with the first electrode of increased surface area. Conventionally, HSG is formed to optimize surface area with very closely positioned grains since a capacitor electrode will consist of the HSG. In the present aspect of the

invention, less closely positioned grains may be formed than would provide optimal surface area for rugged or HSG polysilicon since the first electrode can be formed on the polysilicon rather than consist of the polysilicon. The less closely position grains of the invention will provide a greater outer surface area for the first electrode compared to what HSG optimized for surface area would provide to a first electrode formed on optimized HSG. Also, undoped grains of rugged polysilicon may provide the advantage of grain size being smaller than for doped grains such that a smaller capacitor container may be used.

Figs. 1-6 exemplify the features of the various aspects of the invention described above, as well as other aspects of the invention. For example, according to another aspect of the invention, Fig. 1 shows wafer portion 1 including a substrate 2 with an insulative layer 4 formed thereon. A capacitor fabrication method may include forming an opening 16 in insulative layer 4, the opening 16 having sides and a bottom. Although not shown, the opening may expose an electrical contact in substrate 2 for subsequent electrical linking with a capacitor electrode. Turning to Fig. 2, a layer of polysilicon 6 may be formed over the sides and bottom of the opening. Polysilicon layer 6 may then be removed from over the bottom of opening 16 and converted by low density seeding to an undoped rugged layer 8 comprising HSG polysilicon, as shown in Fig. 3. An anisotropic spacer etch may be used to remove polysilicon, preferably before conversion, from over the bottom of the

opening while leaving polysilicon over the sides. Accordingly, no undoped polysilicon will exist between an electrical contact, such as a polysilicon or metal plug, in substrate 2 and a bottom capacitor electrode. If polysilicon is present at the bottom, it may cause high contact resistance or an open between the bottom electrode and the contact.

In Fig. 4, a first capacitor electrode 10 may be conformally formed on undoped polysilicon 8. First electrode 10 may be sufficiently thin that it has an outer surface area per unit area greater than an outer surface area per unit area of the portion of substrate 2 underlying first electrode 10. For example, first electrode 10 may have a thickness of from about 50 to about 500 Angstroms, preferably about 200 Angstroms. A capacitor dielectric layer 12 may be formed on first electrode 10 as shown in Fig. 5. Fig. 6 shows excess portions of dielectric layer 12 and a subsequently formed second capacitor electrode layer 14 removed from over insulative layer 4 to produce a capacitor construction.

Advantageously, first electrode 10 has an enhanced surface area yet might not produce a SiO_2 interfacial dielectric with an oxygen containing dielectric layer since first electrode 10 may comprise materials other than polysilicon, for example, TiN. Accordingly, the benefits of high K dielectrics, such as Ta_2O_5, may be maximized while still providing enhanced electrode surface area.

Figs. 7-10 exemplify the features of the various aspects of the invention described above pertaining to barrier layers, as well as other aspects of the invention, according to an alternative process flow. For example, Fig. 7 shows wafer portion 1 of Fig. 2 including a substrate 2 with insulative layer 4, opening 16 in insulative layer 4, and polysilicon layer 6 converted to a first capacitor electrode 18 comprising doped HSG polysilicon.

In Fig. 8, a conductive barrier layer 20 may be conformally formed on first electrode 18 by, for example, ALD. A capacitor dielectric layer 22 may be formed on barrier layer 20. The barrier layer may be sufficiently thick and dense to reduce oxidation of electrode 18 by oxygen diffusion from over the barrier layer. One source of oxygen diffusion may be dielectric layer 22. Fig. 9 shows formation of a second capacitor electrode 24 on dielectric layer 22. Fig. 10 shows excess portions of barrier layer 20, dielectric layer 22, and second electrode layer 24 removed from over insulative layer 4 to form a capacitor construction. As described above, a barrier layer may also be formed over a dielectric layer although not shown in the Figures.

In a still further alternative aspect of the invention, barrier layer 20 may be removed from over insulative layer 4 prior to forming dielectric layer 22. Chemical mechanical polishing is one example of a suitable removal method for excess portions of barrier layer 20. However, such an alternative is less preferred since the portion of first

electrode 18 planar with insulative layer 4 might be exposed during polishing and may contact dielectric layer 22. At the point of contact, an SiO_2 interfacial dielectric may form if first electrode 18 includes silicon and dielectric layer 22 includes oxygen.

In compliance with the statute, the invention has been described in language more or less specific as to structural and methodical features. It is to be understood, however, that the invention is not limited to the specific features shown and described, since the means herein disclosed comprise preferred forms of putting the invention into effect. The invention is, therefore, claimed in any of its forms or modifications within the proper scope of the appended claims appropriately interpreted in accordance with the doctrine of equivalents.

CLAIMS:

1. A capacitor fabrication method comprising:

forming a first capacitor electrode over a substrate, the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate;

forming a capacitor dielectric layer over the first electrode; and

forming a second capacitor electrode over the dielectric layer.

2. The method of claim 1 wherein the first electrode comprises TiN.

3. The method of claim 1 further comprising forming rugged polysilicon over the substrate, the first electrode being over the rugged polysilicon.

4. The method of claim 3 wherein the rugged polysilicon is undoped.

5. The method of claim 3 wherein the rugged polysilicon comprises hemispherical grain polysilicon.

6. The method of claim 3 wherein the forming the rugged polysilicon comprises using a seed density sufficiently small to yield at least some spaced apart grains.

7. The method of claim 1 wherein the outer surface area of the first electrode is at least 30% greater than the outer surface area of the substrate.

8. The method of claim 1 wherein the forming the first electrode comprises:

chemisorbing a layer of a first precursor at least one monolayer thick over the substrate;

chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by the first electrode.

9. The method of claim 1 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

10. A capacitor fabrication method comprising:

forming an opening in an insulative layer over a substrate, the opening having sides and a bottom;

forming a layer of polysilicon over the sides and bottom of the opening;

removing the polysilicon layer from over the bottom of the opening;

converting at least some of the polysilicon layer to hemispherical grain polysilicon;

conformally forming a first capacitor electrode on the converted polysilicon, the first electrode being sufficiently thin that the first electrode has an outer surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode;

forming a capacitor dielectric layer on the first electrode; and

forming a second capacitor electrode over the dielectric layer.

11. The method of claim 10 wherein the hemispherical grain polysilicon is undoped.

12. The method of claim 10 wherein the converting the polysilicon comprises using a seed density sufficiently small to yield at least some spaced apart grains.

13. The method of claim 10 wherein the forming the first electrode comprises:

chemisorbing a layer of a first precursor at least one monolayer thick on the converted polysilicon;

chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by the first electrode.

14. The method of claim 10 wherein the first electrode comprises TiN.

15. The method of claim 10 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

16. A capacitor construction comprising:

a first capacitor electrode over a substrate, the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate;

a capacitor dielectric layer over the first electrode; and

a second capacitor electrode over the dielectric layer.

17. The construction of claim 16 wherein the first electrode comprises TiN.

18. The construction of claim 16 further comprising rugged polysilicon over the substrate, the first electrode being over the rugged polysilicon.

19. The construction of claim 18 wherein the rugged polysilicon is undoped.

20. The construction of claim 18 wherein the rugged polysilicon comprises spaced apart grains.

21. The construction of claim 16 wherein the outer surface area of the first electrode is at least 30% greater than the substrate outer surface area.

22. A capacitor construction comprising:

an opening in an insulative layer over a substrate, the opening having sides and a bottom;

a hemispherical grain polysilicon layer over the sides of the opening but not over the bottom;

a conformal first capacitor electrode on the polysilicon, the first electrode being sufficiently thin that the first electrode has a rugged outer surface with an outer surface area per unit area greater than an outer surface area per unit area of the substrate underlying the first electrode;

a capacitor dielectric layer on the first electrode; and

a second capacitor electrode over the dielectric layer.

23. The construction of claim 22 wherein the polysilicon is undoped.

24. The construction of claim 22 wherein the polysilicon comprises spaced apart grains.

25. The construction of claim 22 wherein the first electrode comprises TiN.

26. The construction of claim 22 wherein the dielectric layer comprises Ta_2O_5, ZrO_2, WO_3, Al_2O_3, HfO_2, barium strontium titanate, or strontium titanate.

ABSTRACT OF THE DISCLOSURE

A capacitor fabrication method may include atomic layer depositing a conductive barrier layer to oxygen diffusion over the first electrode. A method may instead include chemisorbing a layer of a first precursor at least one monolayer thick over the first electrode and chemisorbing a layer of a second precursor at least one monolayer thick on the first precursor layer, a chemisorption product of the first and second precursor layers being comprised by a layer of a conductive barrier material. The barrier layer may be sufficiently thick and dense to reduce oxidation of the first electrode by oxygen diffusion from over the barrier layer. An alternative method may include forming a first capacitor electrode over a substrate, the first electrode having an inner surface area per unit area and an outer surface area per unit area that are both greater than an outer surface area per unit area of the substrate. A capacitor dielectric layer and a second capacitor electrode may be formed over the dielectric layer. The method may further include forming rugged polysilicon over the substrate, the first electrode being over the rugged polysilicon. Accordingly, the outer surface area of the first electrode can be at least 30% greater than the outer surface area of the substrate without the first electrode including polysilicon.

MI22-1518

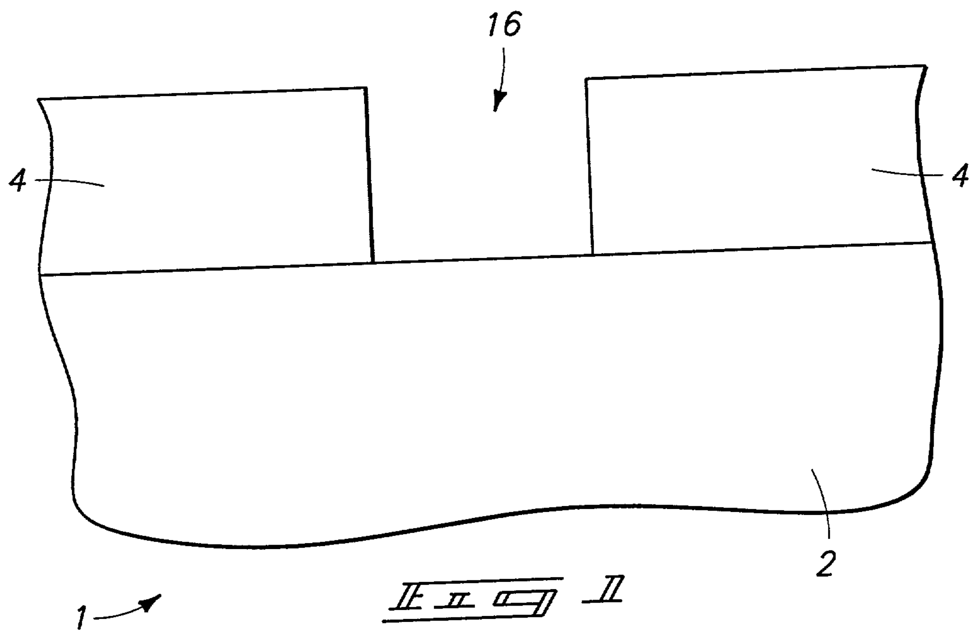


Fig 1

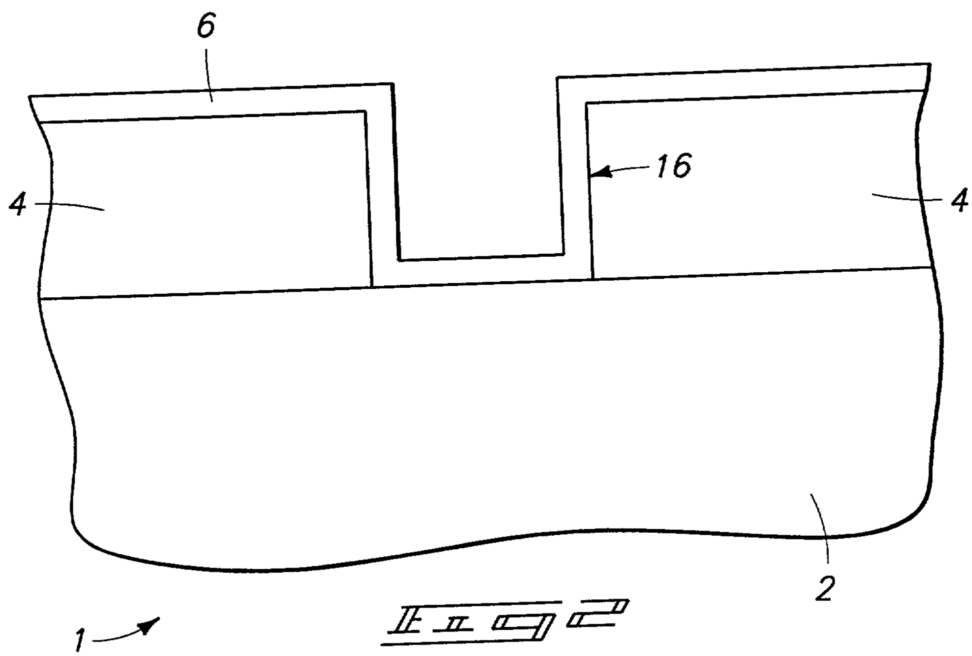
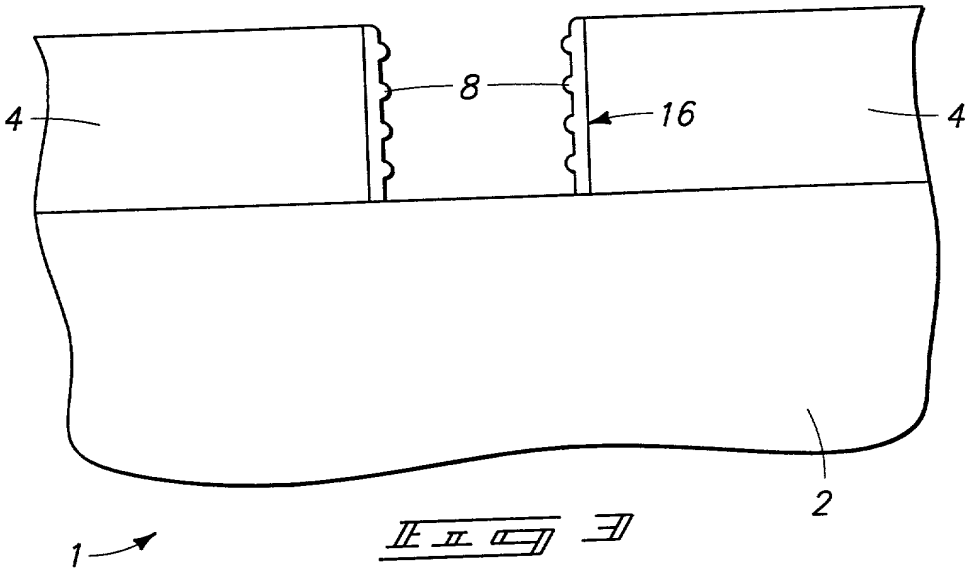
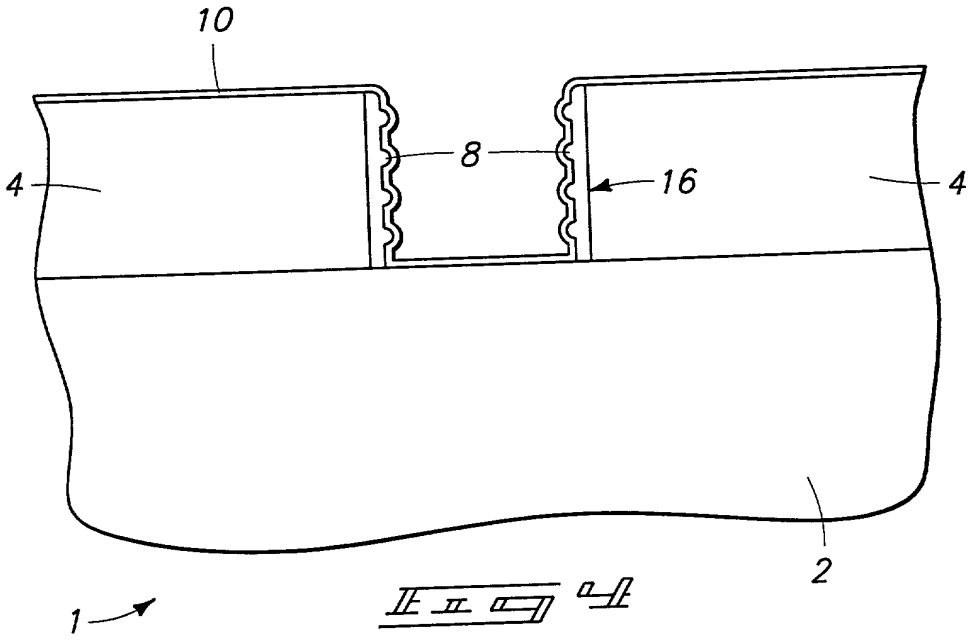


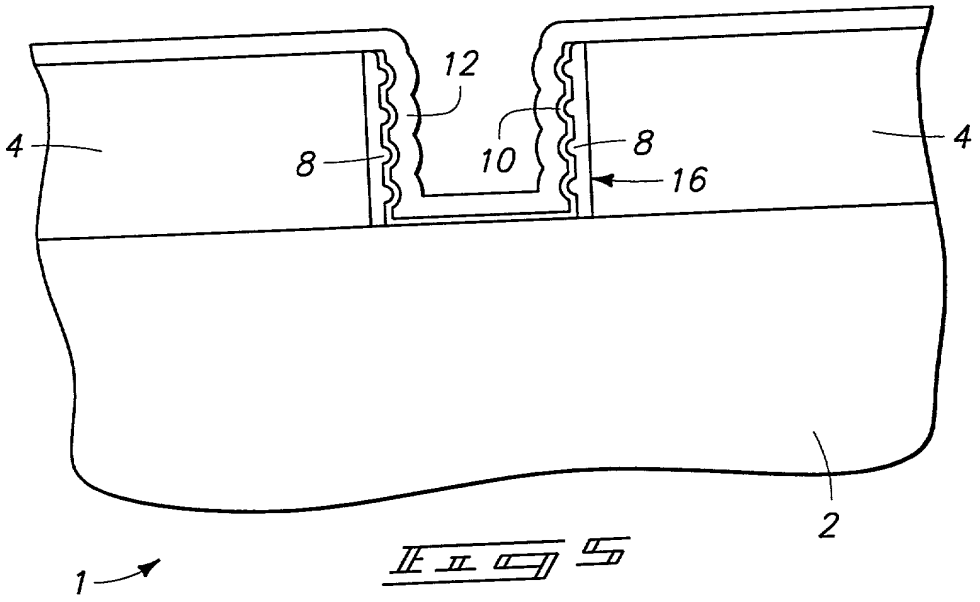
Fig 2



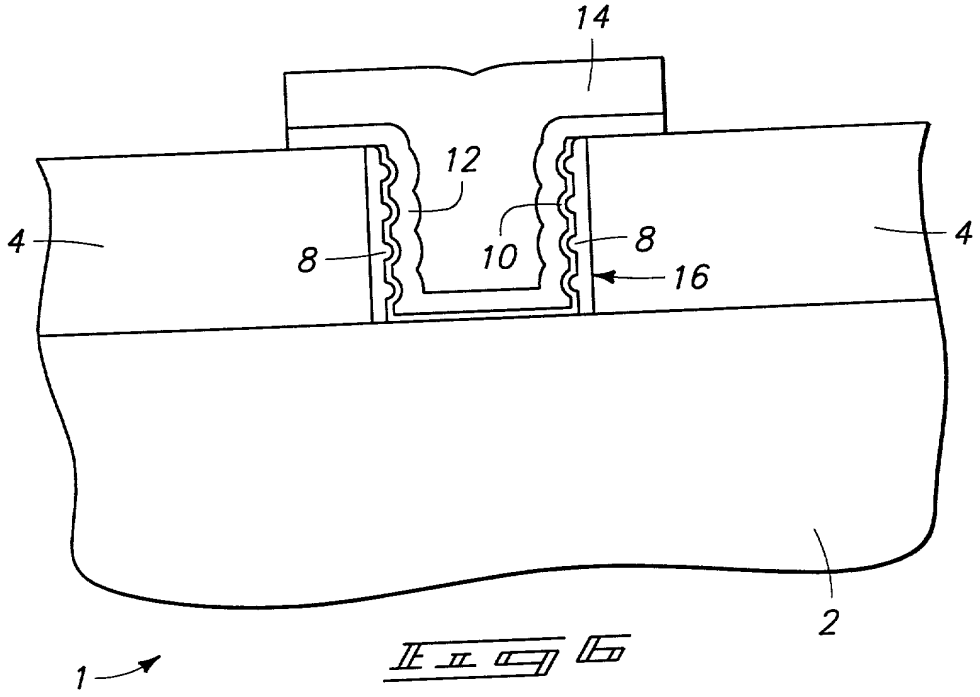
Фиг 3



Фиг 4



Фиг 5



Фиг 6

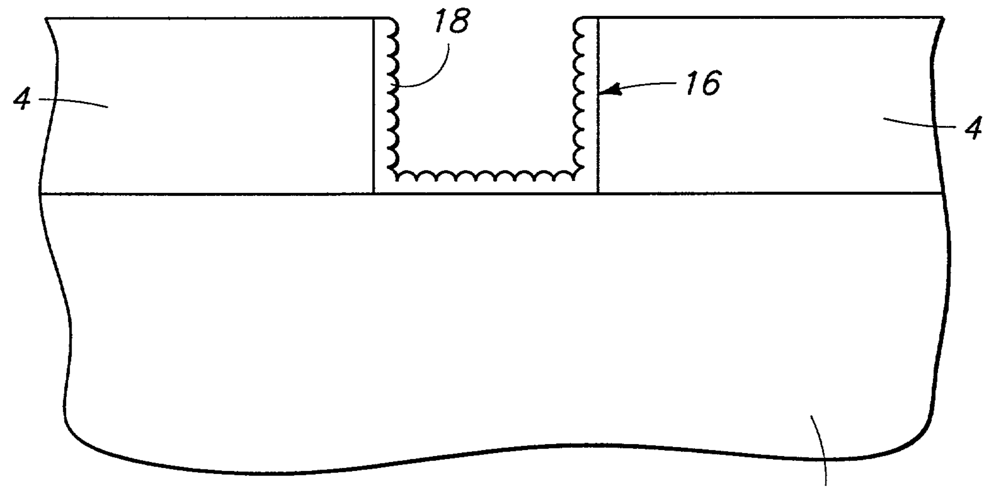


Fig 7

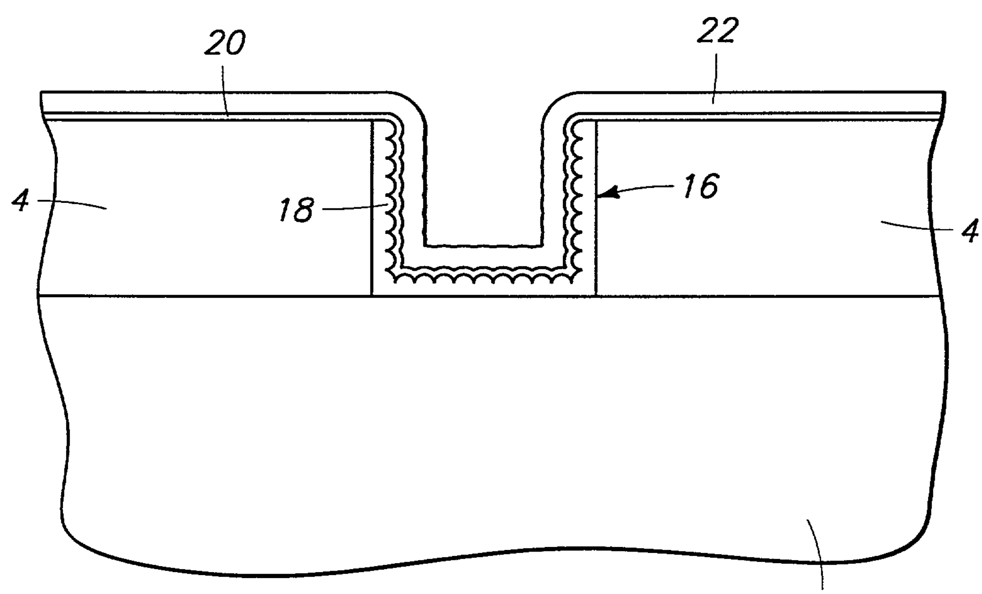
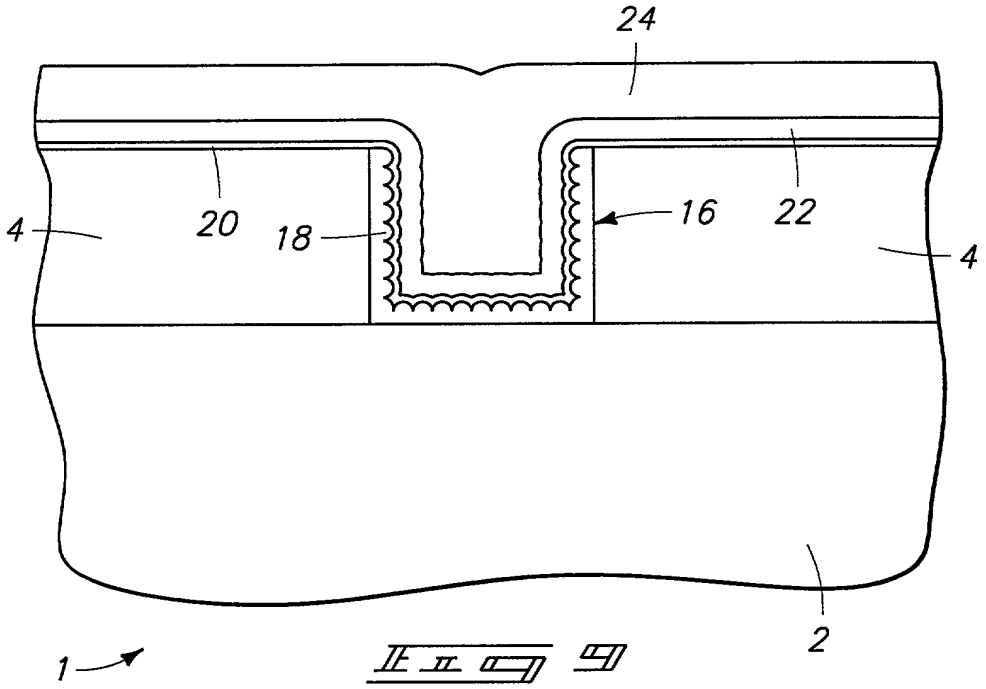
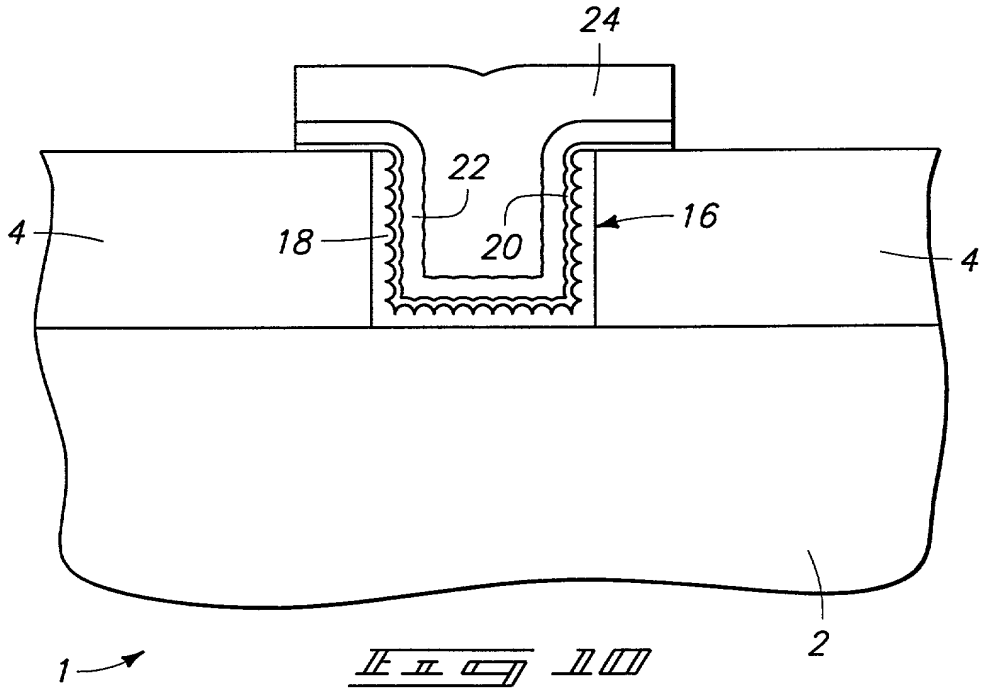


Fig 8



Фиг 9



Фиг 10